

HIGHLY ACCURATE SPURIOUS-FREE INTEGRATED VCO RESONATOR IN A GSM TRANSCEIVER USING CIRCUIT-PACKAGE CO-DESIGN

Jenshan Lin, Ran-Hong Yan, Robert C. Frye, Peter R. Smith, and Yee L. Low

Bell Laboratories, Lucent Technologies
600 Mountain Avenue, Murray Hill, NJ 07974

Abstract

We report an integrated VCO in GSM transceiver with less than 1% frequency error in the first design and spurious-free frequency response. The first-design success with high accuracy is due to considering the package as part of the circuit design and included in optimization. The spurious-free frequency response is achieved by carefully designing a high-Q (37.5@1 GHz) inductor and a co-planar stripline in the VCO resonator.

Introduction

Circuit design and package design have long been considered as two separate entities. A circuit designer usually designs circuits on the chip while specifying the requirements on the package in order to deliver the performance. With the advanced packaging technologies capable of fabricating integrated passive components, however, the package becomes part of the circuit design and can be optimized together. This is particularly beneficial to RF circuits when the package parasitic effect becomes significant. For example, VCO resonator is a high-Q circuit and requires high accuracy in its frequency response. In order to achieve a design with high accuracy, circuit-package co-design must be used to optimize the circuit function by including all the package parasitics and chip characteristics into simulation.

In this paper, we report a design of integrated VCO resonator circuit in a GSM transceiver[1] using thin-film packaging technology. The packaging process is capable of fabricating thin-film resistors, capacitors, inductors, and transmission lines with tight tolerance control [2]. Critical passive circuits, e.g., VCO resonator and impedance matching network, are able to be designed off-chip and integrated in the package. A CMOS RF oscillator circuit based on this

technology was demonstrated[3]. The high-resistivity silicon substrate (>10 K Ω -cm) provides an excellent environment of designing high-Q inductors accurately[4]. In addition to this, flip-chip solder bump assembly reduces the package parasitics of bond wires.

As a result, our design has achieved very high accuracy: the measured 1 GHz VCO frequency is within 1% of predicted value, in the first design iteration. Since the VCO resonator was optimized by circuit-package co-design, it shows a spurious-free response up to 3 GHz. This is an improvement compared to a previous designed VCO resonator for 64-TQFP package where a spurious resonance at 2.2 GHz has caused system-level integration concerns.

VCO Resonator

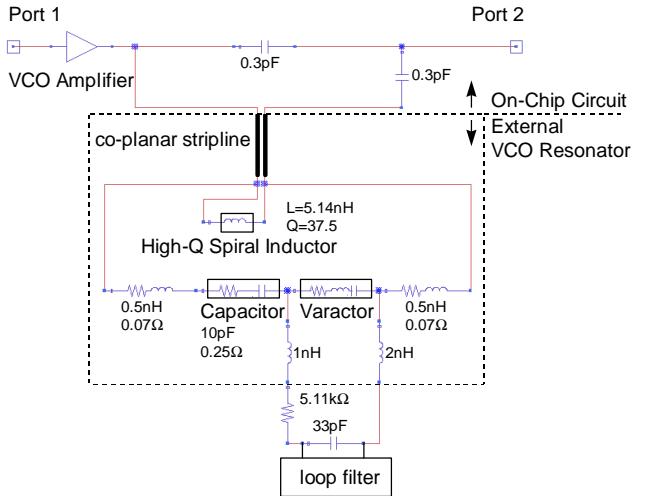


Fig. 1 VCO Circuit Diagram.

The VCO circuit uses a parallel L-C resonator as in Figure 1. The basic part consists of a high-Q spiral inductor and a varactor. A DC-blocking capacitor of

10pF is needed for separating varactor bias from Vcc on the chip. All the parasitic inductance and resistance were considered and included in the design. Loop filter is connected to the varactor through a 5.11 K Ω resistor and 33 pF capacitor external to the package. Since it is very critical to minimize the parasitic effects at the interface between the resonator and the chip, we designed a special co-planar stripline connecting the resonator to the chip to eliminate parasitics.

One of the key design challenges is to have an accurate high-Q spiral inductor in the resonator circuit. Since the tolerance requirement of VCO frequency is 3%, the inductor has to be designed very accurately. The following design considerations are used to ensure the design accuracy of high-Q inductor:

- 1) Two layers of metal were stacked together to reduce the resistance of the inductor. The total metal thickness is 6 μ m.
- 2) The size of inductor, which is about 1 mm², was optimized to have its self-resonant frequency at 4 GHz, and its peak of Q slightly above 1 GHz. The reason for this is to achieve a higher accuracy in predicting inductance at 1 GHz and to avoid spurious resonance.
- 3) To reduce the current crowding effect which degrades inductor Q significantly[4], the spiral inductor was designed with a large opening at center.
- 4) A microstrip inductor model with calibrated substrate characteristics was used to predict the frequency response. The inductor was designed to have an inductance of 5.14 nH and a quality factor over 50 at 1 GHz.

The varactor is a silicon epitaxial planar diode manufactured by Toshiba (1SV239). The varactor is modeled by a series RLC with R=0.7 Ω , L=1.13 nH, and

$$C = 7.0402 - 1.9641 V_{var} + 0.3147 V_{var}^2$$

where V_{var} is the varactor reverse bias voltage. The equation comes from the fitted 2nd order polynomial of measured data between 1 V and 2 V. The variation of varactor capacitance within a wafer lot is much less than 1%.

The co-planar stripline section is crucial to the accurate design. The resonator cannot be placed

arbitrarily close to the chip, and therefore a transmission line section has to be used for connection between resonator and chip to eliminate parasitics. Since the two bond pads for connection to external resonator are very close to each other, a co-planar stripline is chosen. At resonance, the parallel L-C resonator presents a large resistance at the end of co-planar stripline. This special design eliminates undesirable parasitics and therefore increases design accuracy due to the following two reasons:

- 1) The currents on the two lines are out-of-phase and cancel each other in generating parasitic inductance;
- 2) Since the characteristic impedance of co-planar strip line ($\sim 55 \Omega$) is smaller than the resistance of resonator at resonance, the short co-planar stripline section is equivalent to a small shunt capacitance (0.1 pF) across the resonator.

All the parasitics associated with metal trace and passive elements were also considered in the resonator circuit. The two most significant ones are two leads connecting the co-planar stripline to the varactor and the 10 pF capacitor, respectively. They contribute to a total of 1 nH and 0.14 Ω . The 1 nH and 2 nH lead inductances on multi-layer ball-grid-array FR4 board were also included but their effect was greatly reduced by the 5.11 K Ω resistor.

The VCO resonator was optimized by including the on-chip amplifier and feedback network into simulation. The goal is to have the VCO tunable from 996 MHz to 1032 MHz within 1 V to 2 V varactor tuning voltage, and to have a tuning sensitivity around 60 MHz/V. A 2-port S-parameter data extracted from on-chip circuitry was used to model the VCO amplifier. The oscillation frequency is determined by simulating S_{21} of the VCO circuit in Figure 1.

Package Integration

Figure 2 is the photograph of the high-resistivity silicon substrate (7 mm x 7 mm) before mounting the chip and the varactor. The resonator circuit consists of a high-Q inductor, a surface-mount varactor, a 10pF blocking capacitor, and a section of co-planar stripline connecting to the GSM transceiver chip.

The transceiver chip was flip-chip mounted on the substrate on which the VCO resonator was fabricated. Two metal layers of aluminum with a

thickness of 3 μm each were used for high-Q inductors. The substrate has a stable resistivity higher than 10 $\text{K}\Omega\text{-cm}$. The varactor was then mounted on the substrate. The silicon substrate with integrated transceiver chip and VCO resonator circuit was soldered to a multi-layer circuit board with ball-grid array contacts. This module was then ready to be mounted on an evaluation circuit board for functional test.

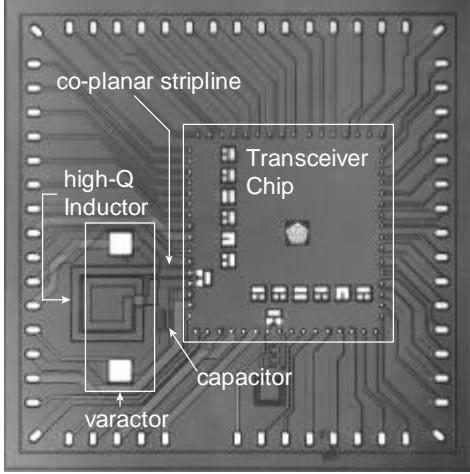


Fig. 2 Photograph of high-resistivity silicon substrate showing VCO resonator circuit and locations of transceiver chip and surface mount varactor.

Measured Performance

The high-Q inductor's frequency response was measured and compared with the simulation. Figure 3 shows both the measured and simulated frequency responses of this high-Q inductor. The error in the inductance at 1 GHz is 3%. The measured self-resonant frequency is slightly lower than 4 GHz. The measured Q at 1 GHz is 37.5 where the peak of Q is 43 at 1.6 GHz. One possible cause of lower Q in measurement is the probe contact resistance with aluminum.

Figure 4a shows the frequency response of the unloaded VCO resonator from 0.5 GHz to 3 GHz, at five different varactor tuning voltages. The response is spurious-free within this band. A spurious resonance at 2.2 GHz of a previously designed VCO resonator using ceramic inductor (Figure 4b) was eliminated. This performance improvement is mainly

due to the carefully designed high-Q inductor and co-planar stripline.

The VCO performance was then measured with the module mounted on an evaluation board and with phase-locked loop filter and bias network in place. Figure 5 compares the measured tuning performance with design simulation. VCO frequency was measured at three varactor bias voltages and the results are all within 1% of predicted value. The averaged tuning sensitivity is 57 MHz/V, which is very close to the designed target 60 MHz/V.

For manufacturing consideration, numbers of samples were measured across wafers and lots. The relative standard deviation (1σ) of resonant frequency is found to be less than 0.5 %.

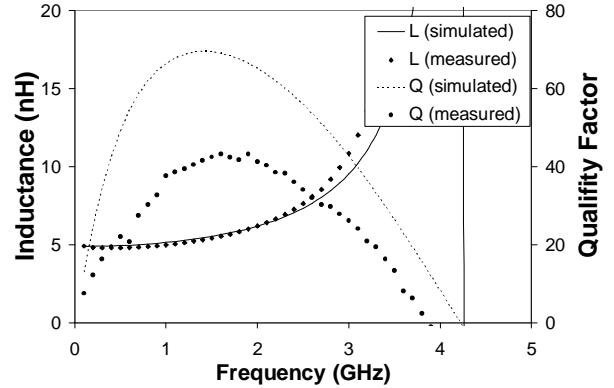


Fig. 3 Frequency response of the high-Q spiral inductor.

Conclusions

We have demonstrated that through circuit-package co-design of the VCO resonator for a GSM transceiver, both high design accuracy and performance improvement were achieved. Fabricated on a high-resistivity silicon substrate, the carefully designed high-Q inductor and co-planar stripline in the VCO resonator eliminate spurious resonance associated with traditional package. The measured VCO frequency from the very first design iteration falls within 1% of designed value across the tuning range. The first design success implies potential savings in both time and cost in circuit development.

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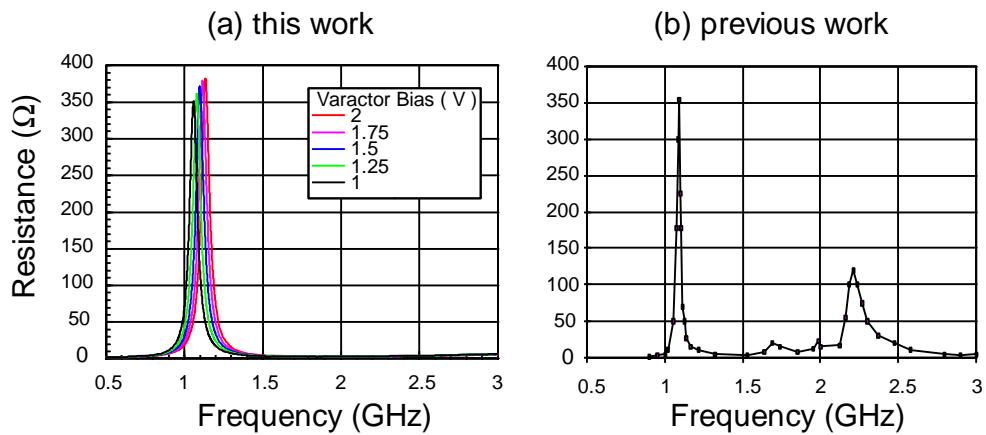


Fig. 4 (a) Measured frequency response of the unloaded resonator circuit at 5 different varactor bias voltages.
 (b) Measured frequency response of a previously designed unloaded resonator circuit using ceramic inductor.

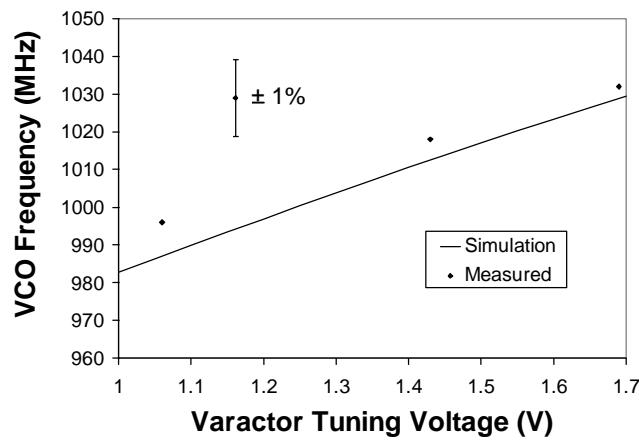


Fig. 5 Comparison of measured VCO tuning performance and simulation.
 Design prediction error is less than 1% throughout VCO tuning range.